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EXAMINER	
HUNG, YUBIN	

ART UNIT	PAPER NUMBER
2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,632	SCHWARTZ, EDWARD L.	
	Examiner	Art Unit	
	Yubin Hung	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *August 30, 2004 & January 18,2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *August 26, 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/16/04 & 5/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment/Arguments

1. This action is in response to amendment and argument filed August 30, 2004 and January 18, 2005.

2. Claims 1-42 are still pending.

3. In view of applicant's amendment, objections to the drawings, the specification and the 35 USC § 112 rejections recited in the previous office action (mailed 02/25/04) have been withdrawn. However, new objection to the drawings has been found; see below.

4. Applicant's arguments filed August 30, 2004 have been fully considered but they are not persuasive; see below.

5. In remarks Applicant argued in substance:

5.1 *that there is no teaching of having an indication indicate* ***in each row of memory the location*** *at which bits of more significant bit planes have started and after which bits of less significant bit planes are no longer stored (P. 14, lines 10-13.)*

However, per the analysis of claim 1 (reproduced below), Yip and Wang in combination teaches storing in a memory only the most significant bit planes (i.e.,

the more significant bit planes are stored, starting, in Yip's case, with the most significant one) of coefficients of which a predetermined number of the least significant bit planes are truncated (i.e., bits of less significant bit planes are not stored). As is well known in the art, and indeed, in the field of computer science in general, to access data (e.g., more significant bit planes) stored in a memory, an addressing mechanism is maintained and used. Abbot expressly disclosed the use of a pointer into a row of memory where a datum of interest (such as the bit values of the most significant bit planes) is stored. Clearly, since a predetermined number of the least significant bit planes have been truncated, they are not stored after the **indicated location in the corresponding memory row**.

5.2 *that one skilled in the art would not look to combine the teachings of Yip, Wang and Abbott to arrive at the present invention as claimed (P. 14, lines 18-20) (because) the feature (described in P. 14, line23 through P. 15, line 2) is clearly not shown in the combination (P. 15, lines 2-3) and that the combination is hindsight because Yip and Wang do not suggest a combination with each other (P. 15, 2nd paragraph).*

However, per the response to argument in 5.1 above, Yip, Wang and Abbott in combination shows the feature described in P. 14, line 23 through P. 15, line 2.

Moreover, In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

One of ordinary skill in the art would have been motivated to combine Wang with Yip as per the analysis of claim 1, because, in addition to the motivation provided therein, Wang further states that by truncating a predetermined number of the least significant bits the memory size and hardware cost are reduced [Col. 2, lines 63-66].

5.3 *that tin the claimed invention there is an embodiment with a counter as described in P. 15, lines 3-6 of the 3rd paragraph (P. 15, 3rd paragraph).*

However, this is irrelevant because such details are not claimed.

Drawings

6. The amended drawings are objected to because Fig. 22A is vague. Specifically, paragraph 0167 of page 72 (where Fig. 22A is described) and the first four lines of paragraph 0168 indicate that 8 bits (presumably indicated by the pairs of numbers, which have not been described, on the leftmost side of Fig. 22A) of each of the 16-bit coefficients are stored in an 8-bit memory location. This being the case, the position in each memory row pointed to by a respective counter (shown by the curve and described in paragraph 0169 on page 73) cannot be the location where the 8 bits are started to be stored since there are fewer than 8 bits to the right of the memory position pointed to by the counter. [Note: However, P. 73, paragraph, 0169 through P. 75, line 5 and Fig. 22B taken together appear to indicate that **all** (say, 16) bits of a coefficient are stored in a memory row and that the counter is used to indicate the start of the needed **N** (say, **N**=8) bits. If this is the case, then the memory reduction stated in paragraph 0167 and shown by Fig. 22A is not achieved.]

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and

where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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Claim Rejections - 35 USC § 103

(From Office Action dated February 25, 2004)

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), in view of Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395)

3. Regarding claim 1, Yip et al. discloses

- applying one or more wavelet transforms to generate a plurality of coefficients [Figs. 1A, 1B, 2, 3; Col. 2, lines 45-62]
- storing the plurality of coefficients in a first memory wherein each storage location in each of the plurality of rows stores a bit of either a more significant bit plane of the plurality of coefficients or a less significant bit plane of the plurality of coefficients
  [Fig. 6, numeral 614; Col. 9, lines 52-57. Note that lines 55-57 indicate that the bit planes are stored in the memory starting with the LSB plane.]

Yip et al. fails to disclose the following, which Wang et al. teaches:

- that only N bit planes of each of the coefficients are to be stored
  [Fig. 1, numeral 40; Col. 2, lines 60-66]

Neither Yip et al. nor Wang et al. discloses the following, which Abbott et al. teaches:

- that the first memory has a plurality of rows

[Col. 6, lines 10-14]

- wherein storing N bit planes includes storing an indication for each row of the plurality of rows to indicate a location in said each row at which bits of more significant bit planes have started to be stored and after which bits of the plurality of coefficients of the less significant bit planes are no longer stored [Abstract: lines 7-10. Note that as stated above, Yip et al. teaches that the bit planes are stored in the memory starting with the LSB plane, and Wang et al. teaches that a predetermined number of LSB planes are not to be needed. The pointer (i.e., indication) therefore can point to the location where the more significant bit planes starts to be stored.]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Yip et al. by not storing a predetermined number of the LSB planes (as taught by Wang et al.), as well as using a plurality of memory rows and for each row also storing an indication to indicate a location in said each row at which bits of more significant bit planes have started to be stored and after which bits of the plurality of coefficients of the less significant bit planes are no longer stored (as taught by Abbott et al.). In this way only the needed (i.e., the more significant bit planes indicated by the pointers) data need to be read from the memory arrays with the added benefit of reduced memory requirement for subsequent processing. In addition, the use of multiple rows also makes the method amenable to parallel processing. Therefore the modifications can greatly improve the processing efficiency.

4. Regarding claim 3, Wang et al. teaches truncating below the N bit planes [Col. 2, lines 60-66].

5. Regarding claim 13, in addition to teaching the use of pointers to indicate locations at which bits of more significant bit planes have started to be stored (as per analysis for claim 1), Abbott et al. also teaches that those pointers (i.e., the indication") point to a memory address [Abstract: line 9].

6. Regarding claim 18, the combined invention of Yip et al., Abbott et al. and Wang et al. teaches everything except expressly the following:

- the plurality of rows comprises eight rows

At the time the invention was made, it would have been to a person of ordinary skill in the art to use eight memory rows. Applicant has not disclosed that using eight memory rows provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with fewer or more number of memory rows because the optimal number of rows to use depends on the size of the data to be stored.

Therefore, it would have been obvious to one of ordinary skill in this art to modify the combined invention of Yip et al., Abbott et al. and Wang et al. by using eight memory rows to obtain the invention as specified in claim 18.

7. Regarding claim 21, Abbott et al. further teaches the use of a second memory for the pointers (i.e., the "indications"). [Fig. 3.]

8. Claims 22, 24, 34, 39, 42, being the apparatus claims for the respective method claims 1, 3, 13, 18, 21, are similarly analyzed and rejected.

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9. Claims 2, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395) as applied to claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 above, and further in view of Yip et al. (US 6,266,450, hereinafter refers to as Yip-2).

10. Regarding claim 2, the combined invention of Yip et al., Abbott et al. and Wang et al. fails to teach the following, which Yip-2 teaches:

- storing of the plurality of coefficients occurs prior to identification of the number of zero bit planes in the plurality of coefficients
  [Fig. 36, numerals 3602-3606; Col. 20, line 63-Col. 21, line 14]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. and Wang et al. with the teaching of Yip-2 by storing of the plurality of coefficients prior to identification of the number of zero bit planes in the plurality of coefficients since it is well known in the art that storing of data is an inherently necessary step before they can be operated upon and that zero bit planes can be efficiently encoded (e.g., as the numbers of the zero bit planes).

11. Claim 23, being the apparatus claim for the respective method claim 2, is similarly analyzed and rejected.

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12. Claims 4, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395) as applied to claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 above, and further in view of Linz (US 6,005,901).

13. Regarding claim 4, the combined invention of Yip et al., Abbott et al. and Wang et al. fails to teach the following, which Linz teaches:

- the indication comprises a count
  [Col. 4, lines 7-19]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. and Wang et al. with the teaching of Linz by having a count as part of the indication since memory devices with such capability is commercially available [Linz: Col. 4, line 15-19] and can indicate the current capacity of the memory to receive additional data.

14. Claim 25, being the apparatus claim for the respective method claim 4, is similarly analyzed and rejected.

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15. Claims 5, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634), Wang et al. (US 6,088,395), and Linz (US 6,005,901).as applied to claims 4, 25 above, and further in view of Li (US 6,275,531).

16. Regarding claim 5, the combined invention of Yip et al., Abbott et al., Wang et al. and Linz further teaches that individual counters are associated with only one of the plurality of rows. [Abbott et al. Abstract: lines 7-10.]

The combined invention of Yip et al., Abbott et al. , Wang et al. and Linz fails to teach the following, which Li teaches:

- stopping each counter of the plurality of counters associated with one of the most significant bit planes when a one bit occurs in the one most significant bit plane of a coefficient
  [Col. 7: lines 21-24. Note that the criterion is the existence of at least one non-zero bit, which implies that the counting will necessarily stop when the first such bit is encountered.]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. , Wang et al. and Linz with the teaching of Li by stopping each counter of the plurality of counters associated with one of the most significant bit planes when a 1-bit occurs in

the one most significant bit plane of a coefficient because the object is to determine the most significant bit plane with at least one 1-bit and counting beyond the first such bit only wastes processing time.

17. Claim 26, being the apparatus claim for the respective method claim 5, is similarly analyzed and rejected.

****

18. Claims 6, 8, 27, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395) as applied to claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 above, and further in view of Klassen (US 6,442,302).

19. Regarding claim 6, the combined invention of Yip et al., Abbott et al. and Wang et al. fails to teach the following, which Klassen teaches:

- the indication comprises a variable length code
  [Col. 5, lines 5-8]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. and Wang et al. with the teaching of Klassen by compressing the indications using a variable length coding scheme in order to reduce the data size.

20. Regarding claim 8, Klassen further teaches:

- the variable length code comprises a run length code

  [Col. 5, lines 12-18]

21. Claims 27 and 29, being the apparatus claims for the respective method claims 6 and 8, are similarly analyzed and rejected.

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22. Claims 7, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395), Klassen (US 6,442,302) as applied to claim 6, 8, 27, 29, above, and further in view of Yip-2 (Yip et al. US 6,266,450).

23. Regarding claim 7, the combined invention of Yip et al., Abbott et al., Wang et al. and Klassen fails to teach the following, which Yip-2 teaches:

- the variable length code indicates an amount of bits to skip until a 1-bit is encountered
  [Fig. 36, numerals 3602-3606; Col. 20, line 63-Col. 21, line 14]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al., Wang et al. and Klassen with the teaching of Yip-2 by having the variable length code

indicates an amount of bits to skip until a 1-bit is encountered since a run of 0's can be very efficiently encoded using a variable length coding scheme.

24. Claim 28, being the apparatus claim for the respective method claim 7, is similarly analyzed and rejected.

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25. Claims 9-12, 30-33 rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634), Wang et al. (US 6,088,395), and Klassen (US 6,442,302) as applied to claims 6, 8, 27, 29 above, and further in view of Allen et al. (US 5,381,145).

26. Regarding claims 9, and similarly claim11, the combined invention of Yip et al., Abbott et al., Wang et al., and Klassen fails to teach the following, which Allen et al. teaches:

- the run length code comprises an R2[8] code
  [Col. 10, line 46 - Col. 11, line 14; Table 7.]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al., Wang et al., and Klassen with the teaching of Allen et al. by using R2[8] run length code when

the symbol probability is 0.997 since R2[8] is optimal for this probability, as pointed out by Allen et al. in Table 7.

27. Regarding claim 10, and similarly for claim 12, the combined invention of Yip et al., Abbott et al., Wang et al., and Klassen teaches everything except expressly the following:

- the first memory is 1 /32 the size of a code-block

At the time the invention was made, it would have been to a person of ordinary skill in the art to use a memory with a size 1/32 that of a code-block. Applicant has not disclosed that using a memory with a size 1/32 that of a code-block provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a larger-sized memory, which can reduce code access time (since more are available in the memory), or with a smaller-sized memory, which can lower the memory cost.

Therefore, it would have been obvious to one of ordinary skill in this art to modify the combined invention of Yip et al., Abbott et al., Wang et al., and Klassen by using a memory with a size 1/32 that of a code-block to obtain the invention as specified in claim 10.

28. Claims 30-33, being the apparatus claims for the respective method claims 9-12, are similarly analyzed and rejected.

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29. Claims 14, 15, 17, 35, 36, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395) as applied to claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 above, and further in view of Taubman (US 6,658,159).

30. Regarding claim 14, the combined invention of Yip et al., Abbott et al. and Wang et al. fails to teach the following, which Taubman teaches:

- further comprising a context model accessing coefficients stored in the first memory
  [Col. 6, lines 56-59. Note that the context model for an encoding scheme operating on the coefficients in the first model inherently has to access them in the memory.]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. and Wang et al. with the teaching of Taubman by using a context model accessing coefficients stored in the first memory in order to be able to use an arithmetic encoding scheme to further reduce the size of the coefficients.

31. Regarding claim 15, while the combined invention of Yip et al., Abbott et al., Wang et al., and Taubman does not expressly teach

- the context model generating an address to access a bit in the first memory; and
- comparing the address with a counter value for the bit plane associated with the bit to determine if the bit is data that is not to be used by the context model

It is noted that to access a bit in a memory, it is inherently necessary to generate the corresponding address. It is further noted that since the counter value indicates whether a datum in the memory is to be used by the context model (per the analyses for claims 1 and 14), it is inherently necessary that the generated address needs to be compared with the counter in order not to access un-needed datum.

32. Regarding claim 17, Taubman further teaches the use of a 5/3 (also known as 5,3) wavelet transform. [Col. 15, lines 35-40.]

33. Claims 35, 36, 38, being the apparatus claims for the respective method claims 14, 15, 17, are similarly analyzed and rejected.

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34. Claims 16, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395) as applied to claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 above, and further in view of Chui et al. (US 5,600,373).

35. Regarding claim 16, the combined invention of Yip et al., Abbott et al. and Wang et al. fails to teach the following, which Chui et al. teaches:

- the plurality of coefficients comprises coefficients in other than an LL subband [Fig. 6, numeral 42; Col. 25, lines 28-43]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. and Wang et al. with the teaching of Chui et al. by not including the LL subband because of the observation that most real-world images (such as those of the PGM format) will consist of low-frequency intensities, i.e., the LL subband will contain most of the image content. By not dropping bits from the coefficients in this subband, the loss in image fidelity after encoding can be minimized.

36. Claim 37 being the apparatus claim for the respective method claim 16, is similarly analyzed and rejected.

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37. Claims 19, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395) as applied to claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 above, and further in view of Elrod et al. (US 5,303,200).

38. Regarding claim 19, the combined invention of Yip et al., Abbott et al. and Wang et al. fails to teach the following, which Elrod teaches:

- the more significant bit planes comprise bit planes 8-15 of the plurality of coefficients and the less significant bit planes comprise bit planes 0-7 of the plurality of coefficients
  [Fig. 2, numerals 58a, 58b; Col. 6, lines 12-16]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. and Wang et al. with the teaching of Elrod et al. by dividing the 16 bit planes evenly into the more and the less significant parts to take advantage of the multiple ports afforded the memory in order to improve the memory I/O efficiency.

39. Claim 40, being the apparatus claim for the respective method claim 19, is similarly analyzed and rejected.

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40. Claims 20, 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yip et al. (US 6,606,416), Abbott et al. (US 5,999,634) and Wang et al. (US 6,088,395) as applied to claims 1, 3, 13, 18, 21, 22, 24, 34, 39, 42 above, and further in view of Ammicht et al. (US 6,549,673).

41. Regarding claim 20, the combined invention of Yip et al., Abbott et al. and Wang et al. fails to teach the following, which Ammicht et al. teaches:

- storing the indication in the first memory
  [Fig. 1, numeral 14; Col. 6, line 63-Col. 7, line 6. Note that there is only one memory (the first memory) to store data, including the pointers (i.e., indications)]

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined invention of Yip et al., Abbott et al. and Wang et al. with the teaching of Ammicht et al. by storing the indication in the first memory since it is the only one available.

42. Claim 41, being the apparatus claim for the respective method claim 20, is similarly analyzed and rejected.

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Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yubin Hung whose telephone number is (571) 272-7451. The examiner can normally be reached on 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Yubin Hung
Patent Examiner
April 1, 2005

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